Q u a n t u m D e s i g n



PPMS Application Note 1684-200

Seebeck Artifact in Samples with Strongly Temperature Dependent Resistivity

This application note is relevant to Thermal Transport hardware which involves the AC Transport option (GPIB-based hardware). In the new CAN-based TTO hardware this artifact is not expected to be significant.

The Seebeck effect is the voltage generated across a sample when a temperature drop exists across that sample: $S_{sample} = \Delta V / \Delta T$. However, a voltage can exist across the sample due to bias currents in the voltage amplifier that are passing through the resistive sample and thus contributing to the ΔV measurement. If this "bias voltage" (arising from amplifier bias currents) is constant during the data collection then the differential nature of the Seebeck measurement will reject it and the sample's Seebeck coefficient will be properly reported. An issue arises when this bias voltage varies during the measurement in a way that mimics the Seebeck effect. This can happen when the sample resistance changes due to the heat pulse (i.e., dR/dT is large in magnitude), as is the case for semiconducting materials at low temperature or a sample undergoing a superconducting transition. The equation below combines the sample Seebeck coefficient with an artifact term due to such an effect:

$$S_{reported} = S_{sample} + \frac{I_{bias}}{\Delta T} \cdot \left(T_{avg}^{ON} - T_{avg}^{OFF}\right) \cdot \frac{dR_{sample}}{dT}$$

Where:

 I_{bias} : can be up to ~120 nA in AC Transport hardware

 ΔT : reported Delta Temp. in TTO measurement .DAT file; "temperature drop across sample"

 $T_{avg}^{ON/OFF}$: average sample temperature in heat ON and heat OFF states; "temperature rise of the sample above the bath"

 R_{sample} : sample resistance between V+ and V- leads

For purposes of illustration, we note that in the typical sample $(T_{avg}^{ON} - T_{avg}^{OFF})$ is similar in magnitude to ΔT so these terms may cancel. Taking the ~100 nA figure for I_{bias} and requiring the total artifact term be less than 1 μ V/K (typical noise floor for Seebeck measurements), we find that this requires:

 $|dR/dT| < 10 \ \Omega/K$

in order to neglect the bias current artifact. It may be useful for post processing of data to know that the term $(T_{avg}^{ON} - T_{avg}^{OFF})$ can be rewritten using parameters found in the measurement .DAT file:

$$\begin{pmatrix} T_{avg}^{ON} - T_{avg}^{OFF} \end{pmatrix} = \frac{1}{2} \left(\begin{bmatrix} T_{H}^{ON} - T_{H}^{OFF} \end{bmatrix} + \begin{bmatrix} T_{C}^{ON} - T_{C}^{OFF} \end{bmatrix} \right)$$
$$= \frac{1}{2} \left(TempRise + MaxTemp - map22 - \Delta T \right)$$

Note that *map22* is the cold thermometer baseline, i.e., its average temperature during measurement if no heat had been applied. Consult the TTO User Manual for description of the other quantities.

The .RAW data for the TTO measurement will be helpful in illustrating these thermal properties of the sample as well as the Seebeck bias voltage (it can be positive or negative). This Seebeck artifact has been observed at low temperatures in semiconducting materials with $dR/dT \sim -10$ ohm/K and also at the superconducting transition of other materials. See Figure 1 on the last page for an illustration of this Seebeck artifact in a real cuprate sample.

Mitigation

Try using both gain 125 (enter max Seebeck > 8000 uV) and gain 1000 (enter max Seebeck < 3000 uV) amplifiers as these will have different bias currents. The noise level on gain 125 will be higher but it is instructive to see where the Seebeck vs. *T* curves diverge for the two gain settings.

The bias current in the amplifier may be reduced by adjusting a pot on the board (this R3 setting on the preamp 3084-505 should only be done by QD or under supervision from QD). An adjusted R3 will reduce the bias currents to <10 nA and thus the sensitivity to sample resistance changes is reduced, requiring $|dR/dT| < 100 \Omega/K$.

It is highly recommended to collect sample resistance data so that R(T) and dR/dT can be assessed.



Figure 1: example of a semiconducting sample at low temperatures which shows a temperature dependent Seebeck voltage offset in RAW file (see upper panel) which is due to a sharply increasing sample resistance (lower panel). The resulting reported Seebeck coefficient of up to -4000 uV/K is spurious (lower panel). Note that the X-axis in these graphs is time and the sample temperature is slewing upwards (upper panel).